Docket No. 303.747US1
WD # 448152

Micron Ref. No. 00-1129

Clean Version of Pending Claims

METHOD TO REDUCE TRANSISTOR CHANNEL LENGTH USING SDOX
Applicant: Zhongze Wang et al.
Serial No.: 09/810,005

Claims 1-48 and 54, as of January 21, 2003 (date of response to final office action filed).

1. (Twice amended) A method of reducing a channel length in a transistor, comprising:
forming a gate dielectric layer on a semiconductor substrate;
coupling a barrier layer to the gate dielectric layer, wherein the barrier layer prevents oxide undergrowth;
forming a gate on top of the barrier layer, the gate having sides, and an effective channel length defined by the sides and an amount of overlap between the sides of the gate and a pair of source/drain regions; and
oxidizing the gate with sides of the gate dielectric exposed, wherein a portion of the sides of the gate are converted to an oxide and an effective channel length of the gate is reduced.

2. The method of claim 1, wherein coupling a barrier layer to the gate dielectric layer comprises coupling a silicon nitride (SiN) layer to the gate dielectric layer.

3. The method of claim 2, wherein coupling a silicon nitride (SiN) layer to the gate dielectric layer comprises remote plasma nitride processing to form a silicon nitride (SiN) layer.

4. (Twice amended) The method of claim 1, wherein coupling a barrier layer to the gate dielectric layer comprises composite oxidation processing to form a barrier layer.

5. The method of claim 1, wherein forming a gate dielectric layer on a semiconductor substrate comprises forming a gate oxide layer on a semiconductor substrate.

6. The method of claim 1, wherein forming a gate dielectric layer on a semiconductor substrate comprises forming a gate dielectric layer on a silicon substrate.

C3

7. (Twice amended) A method of forming a transistor, comprising:

forming a first source/drain region and a second source/drain region in a semiconductor substrate;

forming a gate dielectric layer on the semiconductor substrate;

coupling a barrier layer to the gate dielectric layer, wherein the barrier layer prevents oxide undergrowth;

forming a gate on top of the barrier layer, the gate having sides, and an effective channel length defined by the sides; and

oxidizing the gate with sides of the gate dielectric exposed, wherein a portion of the sides of the gate are converted to an oxide and an effective channel length of the gate is reduced.

8. The method of claim 7, wherein coupling a barrier layer to the gate dielectric layer comprises coupling a silicon nitride (SiN) layer to the gate dielectric layer.

9. The method of claim 8, wherein coupling a silicon nitride (SiN) layer to the gate dielectric layer comprises remote plasma nitride processing to form a silicon nitride (SiN) layer.

C4

10. (Twice amended) The method of claim 7, wherein coupling a barrier layer to the gate dielectric layer comprises composite oxidation processing to form a barrier layer.

11. The method of claim 7, wherein forming a gate dielectric layer on a semiconductor substrate comprises forming a gate oxide layer on a semiconductor substrate.

12. The method of claim 7, wherein forming a gate dielectric layer on a semiconductor substrate comprises forming a gate dielectric layer on a silicon substrate.

13. The method of claim 7, further including forming a first source/drain extension adjacent the first source/drain region and a second source/drain extension adjacent the second source/drain region.

C5

14. (Twice amended) A method of forming a transistor, comprising:

forming a first source/drain region and a second source/drain region in a semiconductor substrate;

forming a gate dielectric layer on the semiconductor substrate;

coupling a nitride layer to the gate dielectric layer, wherein the nitride layer prevents oxide undergrowth;

forming a gate on top of the nitride layer, the gate having sides, and an effective channel length defined by the sides; and

oxidizing the gate with sides of the gate dielectric exposed, wherein a portion of the sides of the gate are converted to an oxide and an effective channel length of the gate is reduced.

15. The method of claim 14, wherein coupling a nitride layer to the gate dielectric layer comprises coupling a silicon nitride (SiN) layer to the gate dielectric layer.

16. The method of claim 15, wherein coupling a silicon nitride (SiN) layer to the gate dielectric layer comprises remote plasma nitride processing to form a silicon nitride ~~(SiN) layer.~~

C6

17. (Twice amended) The method of claim 14, wherein coupling a barrier layer to the gate dielectric layer comprises composite oxidation processing to form a barrier layer.

18. The method of claim 14, wherein forming a gate dielectric layer on a semiconductor substrate comprises forming a gate oxide layer on a semiconductor substrate.

19. The method of claim 14, wherein forming a gate dielectric layer on a semiconductor substrate comprises forming a gate dielectric layer on a silicon substrate.

20. The method of claim 14, further including forming a first source/drain extension adjacent the first source/drain region and a second source/drain extension adjacent the second source/drain region.

21. (Twice amended) A method of forming an integrated circuit, comprising:

forming a number of transistors on a semiconductor substrate, wherein forming at least one of the number of transistors comprises:

forming a first source/drain region and a second source/drain region in the semiconductor substrate;

forming a gate dielectric layer on the semiconductor substrate;

coupling a barrier layer to the gate dielectric layer, wherein the barrier layer prevents oxide undergrowth;

forming a gate on top of the barrier layer, the gate having sides, and an effective channel length defined by the sides;

oxidizing the gate with sides of the gate dielectric exposed, wherein a portion of the sides of the gate are converted to an oxide and an effective channel length of the gate is reduced; and

electrically connecting the number of transistors.

22. The method of claim 21, wherein coupling a barrier layer to the gate dielectric layer comprises coupling a silicon nitride (SiN) layer to the gate dielectric layer.

23. The method of claim 22, wherein coupling a silicon nitride (SiN) layer to the gate dielectric layer comprises remote plasma nitride processing to form a silicon nitride (SiN) layer.

C8

24. (Twice amended) The method of claim 21, wherein coupling a barrier layer to the gate dielectric layer comprises composite oxidation processing to form a barrier layer.

25. The method of claim 21, wherein forming a gate dielectric layer on a semiconductor substrate comprises forming a gate oxide layer on a semiconductor substrate.

26. The method of claim 21, wherein forming a gate dielectric layer on a semiconductor substrate comprises forming a gate dielectric layer on a silicon substrate.

C9

27. (Twice amended) A method of forming an integrated circuit, comprising:

forming a number of transistors on a semiconductor substrate, wherein forming at least one of the number of transistors comprises:

forming a first source/drain region and a second source/drain region in the semiconductor substrate;

forming a first source/drain extension adjacent the first source/drain region and a second source/drain extension adjacent the second source/drain region;

forming a gate dielectric layer on the semiconductor substrate;

coupling a barrier layer to the gate dielectric layer, wherein the barrier layer prevents oxide undergrowth;

forming a gate on top of the barrier layer, the gate having sides, and an effective channel length defined by the sides;

oxidizing the gate with sides of the gate dielectric exposed, wherein a portion of the sides of the gate are converted to an oxide and an effective channel length of the gate is

reduced; and

electrically connecting the number of transistors.

Cont C4 D1

28. (Twice amended) A method of forming an integrated circuit, comprising:

forming a number of transistors on a semiconductor substrate, wherein forming at least one of the number of transistors comprises:

forming a first source/drain region and a second source/drain region in the semiconductor substrate;

forming a gate dielectric layer on the semiconductor substrate;

coupling a nitride layer to the gate dielectric layer, wherein the nitride layer prevents oxide undergrowth;

forming a gate on top of the nitride layer, the gate having sides, and an effective channel length defined by the sides;

oxidizing the gate with sides of the gate dielectric exposed, wherein a portion of the sides of the gate are converted to an oxide and an effective channel length of the gate is reduced; and

electrically connecting the number of transistors.

29. The method of claim 28, wherein coupling a nitride layer to the gate dielectric layer comprises coupling a silicon nitride (SiN) layer to the gate dielectric layer.

30. The method of claim 29, wherein coupling a silicon nitride (SiN) layer to the gate dielectric layer comprises remote plasma nitride processing to form a silicon nitride (SiN) layer.

C10 D1

31. (Twice amended) The method of claim 28, wherein coupling a barrier layer to the gate dielectric layer comprises composite oxidation processing to form a barrier layer.

32. The method of claim 28, wherein forming a gate dielectric layer on a semiconductor substrate comprises forming a gate oxide layer on a semiconductor substrate.

33. The method of claim 28, wherein forming a gate dielectric layer on a semiconductor substrate comprises forming a gate dielectric layer on a silicon substrate.

34. The method of claim 28, further including forming a first source/drain extension adjacent the first source/drain region and a second source/drain extension adjacent the second source/drain region.

C4

35. (Twice amended) A method of forming a memory device, comprising:

forming a number of transistors on a semiconductor substrate, comprising:

forming a first source/drain region and a second source drain region in the semiconductor substrate;

forming a gate dielectric layer on the semiconductor substrate;

coupling a barrier layer to the gate dielectric layer, wherein the barrier layer prevents oxide undergrowth;

forming a gate on top of the barrier layer, the gate having sides, and an effective channel length defined by the sides;

oxidizing the gate with sides of the gate dielectric exposed, wherein a portion of the sides of the gate are converted to an oxide and an effective channel length of the gate is reduced;

forming a number of wordlines coupled to the gates of the number of transistors; and

forming a number of bitlines coupled to the first source/drain region of the number of transistors.

36. The method of claim 35, wherein coupling a barrier layer to the gate dielectric layer comprises coupling a silicon nitride (SiN) layer to the gate dielectric layer.

37. The method of claim 36, wherein coupling a silicon nitride (SiN) layer to the gate dielectric layer comprises remote plasma nitride processing to form a silicon nitride (SiN) layer.

C12 01

38. (Twice amended) The method of claim 35, wherein coupling a barrier layer to the gate dielectric layer comprises composite oxidation processing to form a barrier layer.

39. The method of claim 35, wherein forming a gate dielectric layer on a semiconductor substrate comprises forming a gate oxide layer on a semiconductor substrate.

40. The method of claim 35, wherein forming a gate dielectric layer on a semiconductor substrate comprises forming a gate dielectric layer on a silicon substrate.

C13 01

41. (Twice amended) A method of forming a memory device, comprising:

forming a number of transistors on a semiconductor substrate, comprising:

forming a first source/drain region and a second source drain region in the semiconductor substrate;

forming a first source/drain extension adjacent the first source/drain region and a second source/drain extension adjacent the second source/drain region;

forming a gate dielectric layer on the semiconductor substrate;

coupling a barrier layer to the gate dielectric layer, wherein the barrier layer prevents oxide undergrowth;

forming a gate on top of the barrier layer, the gate having sides, and an effective channel length defined by the sides;

oxidizing the gate with sides of the gate dielectric exposed, wherein a portion of

the sides of the gate are converted to an oxide and an effective channel length of the gate is reduced;

forming a number of wordlines coupled to the gates of the number of transistors; and

forming a number of bitlines coupled to the first source/drain region of the number of transistors.

Cont C13 D1

42. (Twice amended) A method of making an information handling system, comprising:

providing a processor chip;

forming a semiconductor memory device, comprising:

forming a number of transistors on a semiconductor substrate, comprising:

forming a first source/drain region and a second source/drain region in the semiconductor substrate;

forming a gate dielectric layer on the semiconductor substrate;

coupling a barrier layer to the gate dielectric layer, wherein the barrier layer prevents oxide undergrowth;

forming a gate on top of the barrier layer, the gate having sides, and an effective channel length defined by the sides;

oxidizing the gate with sides of the gate dielectric exposed, wherein a portion of the sides of the gate are converted to an oxide and an effective channel length of the gate is reduced;

forming a number of wordlines coupled to the gates of the number of transistors;

forming a number of bitlines coupled to the first source/drain region of the number of transistors; and

coupling the processor chip to the semiconductor memory device with a system bus.

43. The method of claim 42, wherein coupling a barrier layer to the gate dielectric layer comprises coupling a silicon nitride (SiN) layer to the gate dielectric layer.

44. The method of claim 43, wherein coupling a silicon nitride (SiN) layer to the gate dielectric layer comprises remote plasma nitride processing to form a silicon nitride (SiN) layer.

C14

45. (Twice amended) The method of claim 42, wherein coupling a barrier layer to the gate dielectric layer comprises composite oxidation processing to form a barrier layer.

46. The method of claim 42, wherein forming a gate dielectric layer on a semiconductor substrate comprises forming a gate oxide layer on a semiconductor substrate.

47. The method of claim 42, wherein forming a gate dielectric layer on a semiconductor substrate comprises forming a gate dielectric layer on a silicon substrate.

48. The method of claim 42, further including forming a first source/drain extension adjacent the first source/drain region and a second source/drain extension adjacent the second source/drain region.

C15 D1

54. (Twice amended) A transistor formed by the following process:

forming a first source/drain region and a second source/drain region in a semiconductor substrate;

forming a gate dielectric layer on the semiconductor substrate;

coupling a barrier layer to the gate dielectric layer, wherein the barrier layer prevents oxide undergrowth;

forming a gate on top of the barrier layer, the gate having sides, and an effective channel length defined by the sides; and

oxidizing the gate with sides of the gate dielectric exposed, wherein a portion of the sides of the gate are converted to an oxide and an effective channel length of the gate is reduced.